SGS-THOMSON MICROELECTRONICS

UNDERSTANDING POWER FACTOR

by L. Wuidart

IF YOU THINK THAT POWER FACTOR IS ONLY COS φ, THINK AGAIN !

The big majority of Electronics designers do not worry about Power Factor (P.F.)

P.F. is something you learnt one day at school in your Electrotechnics course"as being cos φ.

This conventional definition is only valid when considering IDEAL Sinusoidal signals for both current and voltage waveforms.

But the reality is something else, because most off-line power supplies draw a non-sinusoidal current!

Many off-line systems have a typical front-end section made by a rectification bridge and an input filter capacitor.

This front-end section acts as a peak detector (see figure 1).

A current flows to charge the capacitor only when the istantaneous AC voltage exceeds the voltage on the capacitor.

A single phase off-line supply draws a current pulse during a small fraction of the half-cycle duration.

Between those current peaks, the load draws the energy stored inside the input capacitor. The phase lag φ but also the harmonic content of such a typical pulsed current waveform produce non efficient extra RMS currents, affecting then the real power available from the mains.

So, P.F. is much more than simply cos φ!

The P.F. value measures how much the mains efficiency is affected by BOTH phase lag φ AND harmonic content of the input current.

In this context, the standard European project

Figure 1: Full Wave Bridge Rectifier Waveforms.

D95IN223
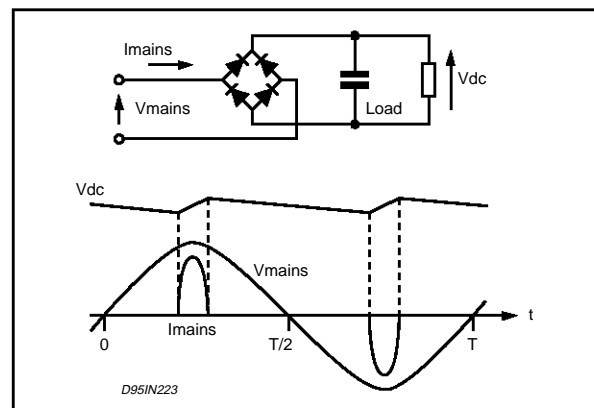
IEC555-2 only defines the current harmonic content limits of mains supplied equipments.
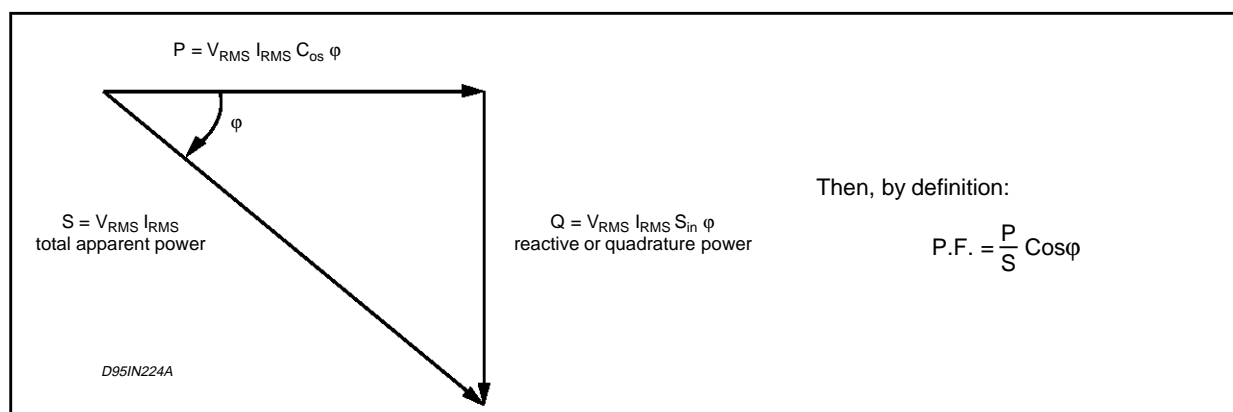
THEORETICAL MEANING

The power factor (P.F.) is defined by:

$$P.F. = \frac{P}{S} = \frac{\text{REAL POWER}}{\text{TOTAL APPARENT POWER}}$$

Ideal Sinusoidal Signals

Both current and voltage waveforms are assumed to be IDEAL SINUSOIDAL waveforms. If the phase difference between the input voltage and the current waveforms is defined as the phase lag angle or displacement angle, the corresponding graphical representation of power vectors gives:

The corresponding power give:

$P = V_{RMS} \, I_{RMS} \, C_{os} \, \varphi$

$S = V_{RMS} \, I_{RMS}$
total apparent power

$Q = V_{RMS} \, I_{RMS} \, S_{in} \, \varphi$
reactive or quadrature power

Then, by definition:

$$P.F. = \frac{P}{S} \, Cos\varphi$$

D95IN224A

Non-ideal sinusoidal current waveform

Assume that the mains voltage is an IDEAL SINUSOIDAL voltage waveform.
Its RMS value is:

$$V_{RMS} = \frac{V_{peak}}{\sqrt{2}}$$

If the current has a periodic non-ideal sinusoidal waveform, the FOURIER transform can be applied

$$I_{RMS}\ total = \sqrt{I_O^2 + I^2{}_{1RMS} + I^2{}_{2RMS} + ... + I^2{}_{nRMS}}$$

Where IO is the DC component of the current, I_{1rms} the fundamental of the RMS current and I_{2RMS} ....I_{nRMS} the harmonics

For a pure AC signal:

$$I_O = 0$$

The fundamental of the RMS current has an in-phase component I_{1RMSP} and a quadrature component I_{1RMSQ}.
So, the RMS current can be espressed as:

$$I_{RMS}\ total = \sqrt{I^2{}_{1RMS}\ P + I^2{}_{1RMS}\ Q + \sum_{n=2}^{\infty} I^2{}_{nRMS}}$$

Then, the Real Power is given by:

$$P = V_{RMS} \cdot I_{1RMS\ P}$$

As φ_1 is the displacement angle between the input voltage and the in-phase component of the fundamental current:

$$I_{1RMS\ P} = I_{1RMS}\ Cos\varphi_1$$

and

$$P = V_{RMS} \cdot I_{1RMS} \cdot Cos\varphi_1$$

$$S = V_{RMS} \cdot I_{RMS\ total}$$

Then, the Power Factor can be calculated as:

$$P.F. = \frac{P}{S} = \frac{I_{1RMS} \cdot Cos\varphi 1}{I_{RMS\ total}}$$

One can introduce the k factor by

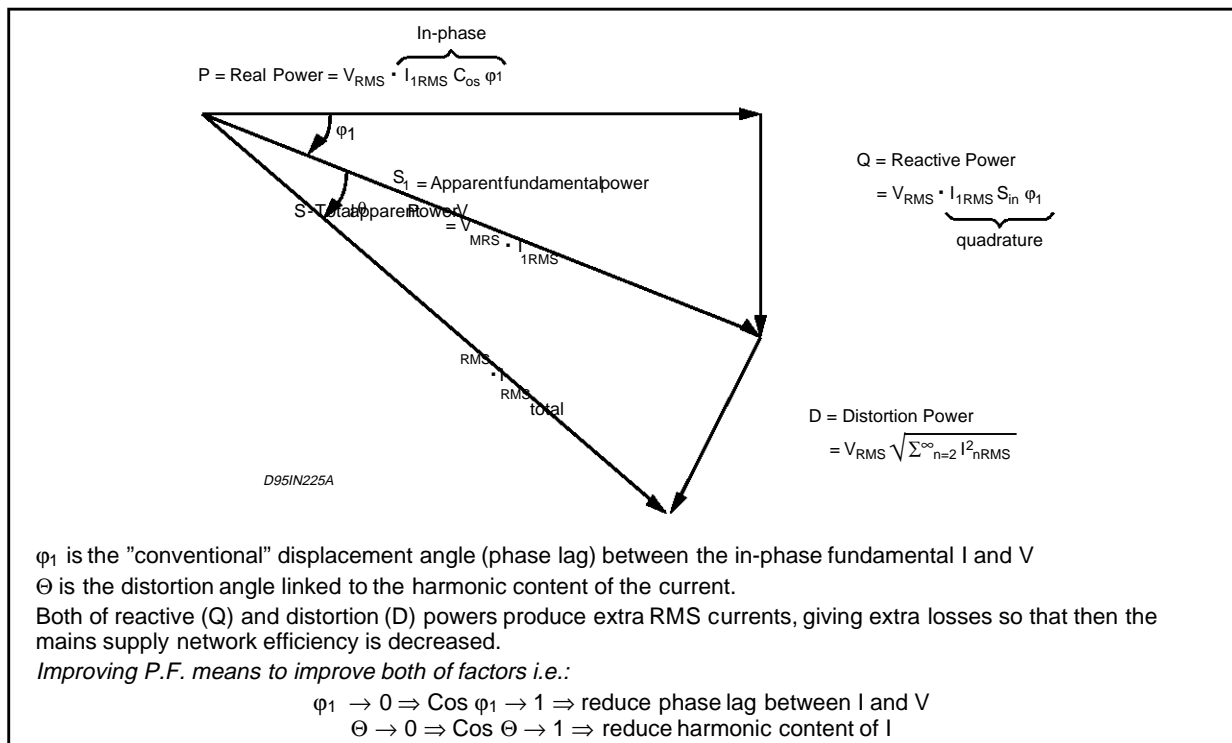$$k = \frac{I_{1RMS}}{I_{RMS\ total}} = Cos\Theta$$

Θ is the distortion angle. The k factor is linked to the harmonic content of the current. If the harmonic content of $I_{RMS\ total}$ is approaching zero, k------> 1.

Conclusion

Finally P.F. can be expressed by:

P.F. = $Cos\Theta \cdot Cos\ \varphi_1$

So, the power vectors representation becomes

P = Real Power = $V_{RMS} \cdot I_{1RMS}\ C_{os}\ \varphi_1$ (In-phase)

S_1 = Apparent fundamental power

S = Total apparent power = $V_{MRS} \cdot I_{1RMS}$

$\cdot I_{RMS\ total}$

Q = Reactive Power
= $V_{RMS} \cdot I_{1RMS}\ S_{in}\ \varphi_1$ (quadrature)

D = Distortion Power
= $V_{RMS} \sqrt{\Sigma^{\infty}_{n=2}\ I^2{}_{nRMS}}$

D95IN225A

φ_1 is the "conventional" displacement angle (phase lag) between the in-phase fundamental I and V
Θ is the distortion angle linked to the harmonic content of the current.
Both of reactive (Q) and distortion (D) powers produce extra RMS currents, giving extra losses so that then the mains supply network efficiency is decreased.
Improving P.F. means to improve both of factors i.e.:

$\varphi_1 \rightarrow 0 \Rightarrow Cos\ \varphi_1 \rightarrow 1 \Rightarrow$ reduce phase lag between I and V
$\Theta \rightarrow 0 \Rightarrow Cos\ \Theta \rightarrow 1 \Rightarrow$ reduce harmonic content of I

SGS-THOMSON
MICROELECTRONICS

PRACTICAL MEANING

The unity power factor beneficiaries

Both of the user and the Electricity distribution company take advantage from a unity power factor. Moreover, adding a PFC brings components cost reduction in the downstream converter.

The user's benefit

At minimum line voltage (85V$_{AC}$), a standard 115V$_{AC}$ well socket should be able to deliver the nominal 15A to a common load.
In similar conditions, a "non-corrected power factor" SMPS (typical value of 0.6) drops the available current from 15A to only 9A.
For example, from one wall socket, four 280W computers each equipped with P.F.C. can be supplied instead of two with no P.F.C.

The Electricity distribution company benefit

Both of reactive (Q) power and distortion (D) power produce extra RMS currents.

The resulting extra losses significantly decrease the mains supply network efficiency. This leads to oversize the copper area of distribution power wires (see figure 3)

The distortion power is linked to the current harmonic content. Delivering power at other frequencies than the line frequency causes a lot of drawbacks.

The current distortion disturbs the zero crossing detection systems, generates overcurrent in the neutral line and resonant overvoltages.

In Europe, the standard EN 60555 and the international project IEC 555-2 limit the current harmonic content of mains supplied equipments.

Figure 2: Reactive and distortion power produce extra RMS currents leading to copper area oversize.
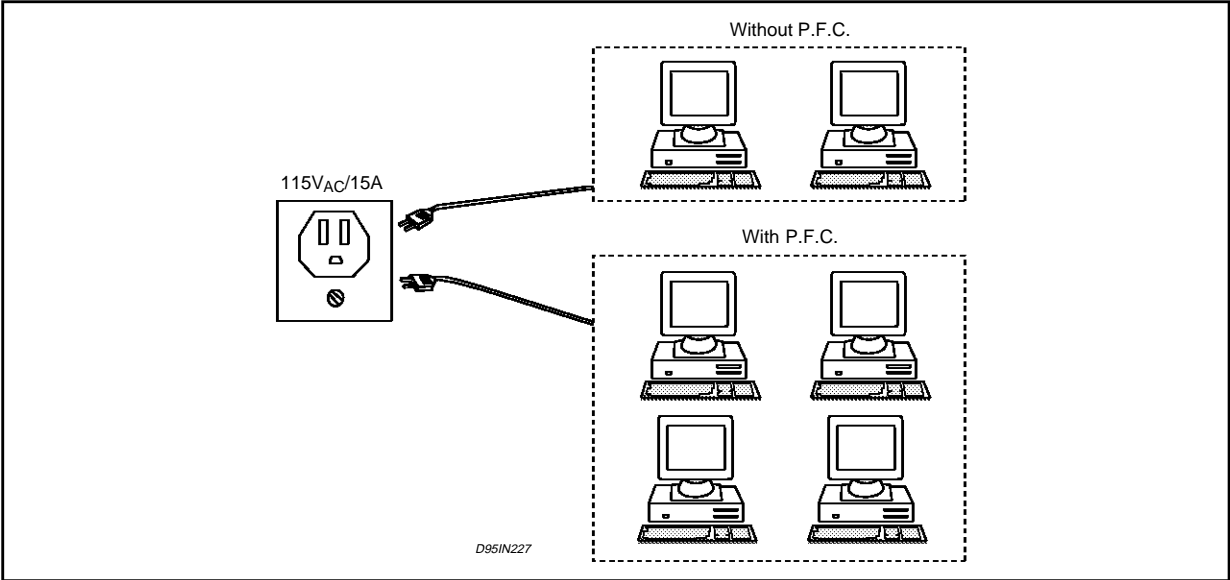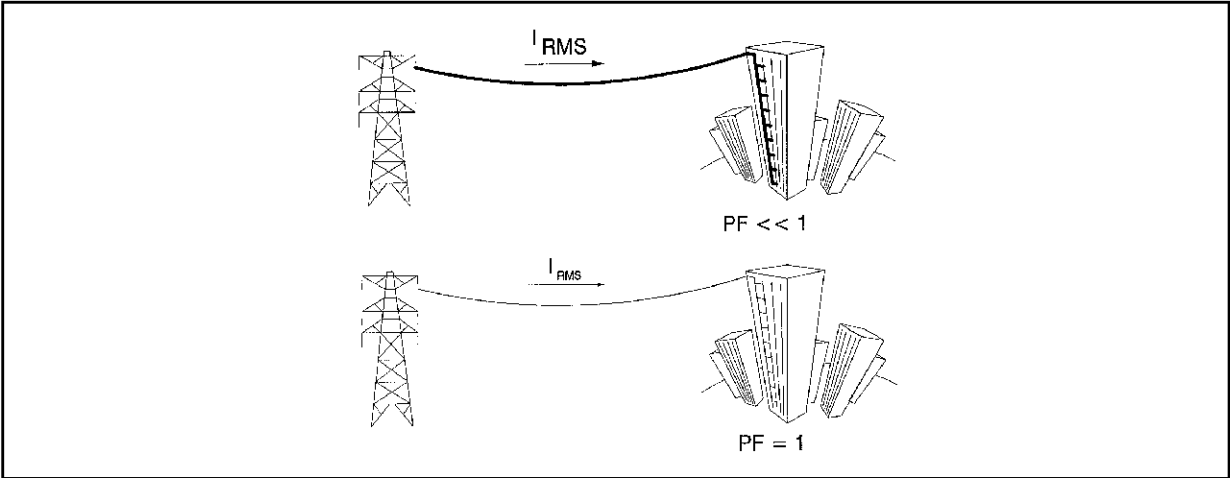

Figure 3: Reactive and distortion power produce extra RMS currents leading to copper area oversize.
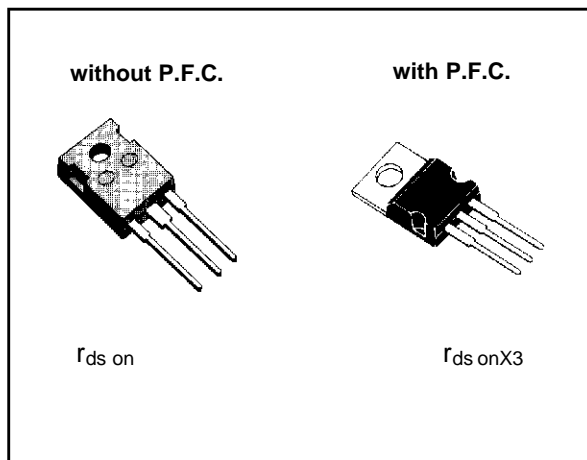
Components cost reduction in the downstream converter

For the same output power capability, a conventional converter using a input mains voltage doubler, is penalized by a 1,8 times higher primary RMS current than with a PFC preregulator.

Consequently, the PFC allows to select power MOSFET's switches with up to 3 times higher on resistance ($r_{ds\ on}$) in the downstream converter (see figure 4).

The converter transformer size can be optimized not only because the copper area is smaller but also, due to the regulated DC bulk voltage delivered by the PFC preregulator.

The PFC provides an automatic mains selection on a widerange voltage from $85V_{AC}$ up to $265V_{AC}$. Compared to the conventional doubler front-end section, the same "hold-up" time can be achieved with a 6 times smaller bulk storage capacitor.

To get 10ms hold-up time, a 100W converter in doubler operation requires a series combination of two $440\mu F$ capacitos instead of one $130\mu F$ with PFC.

Figure 4: Power MOSFET On-resistance (rds on) is 3 times higher by using a PFC.

without P.F.C.   **with P.F.C.**

$r_{ds\ on}$ $r_{ds\ on}X3$

General comments

For new developments, SMPS designers will have to consider the IEC 555-2 standard.

In the practice, this leads to use a PFC is compensated by significant component cost reduction in the downstream converter.
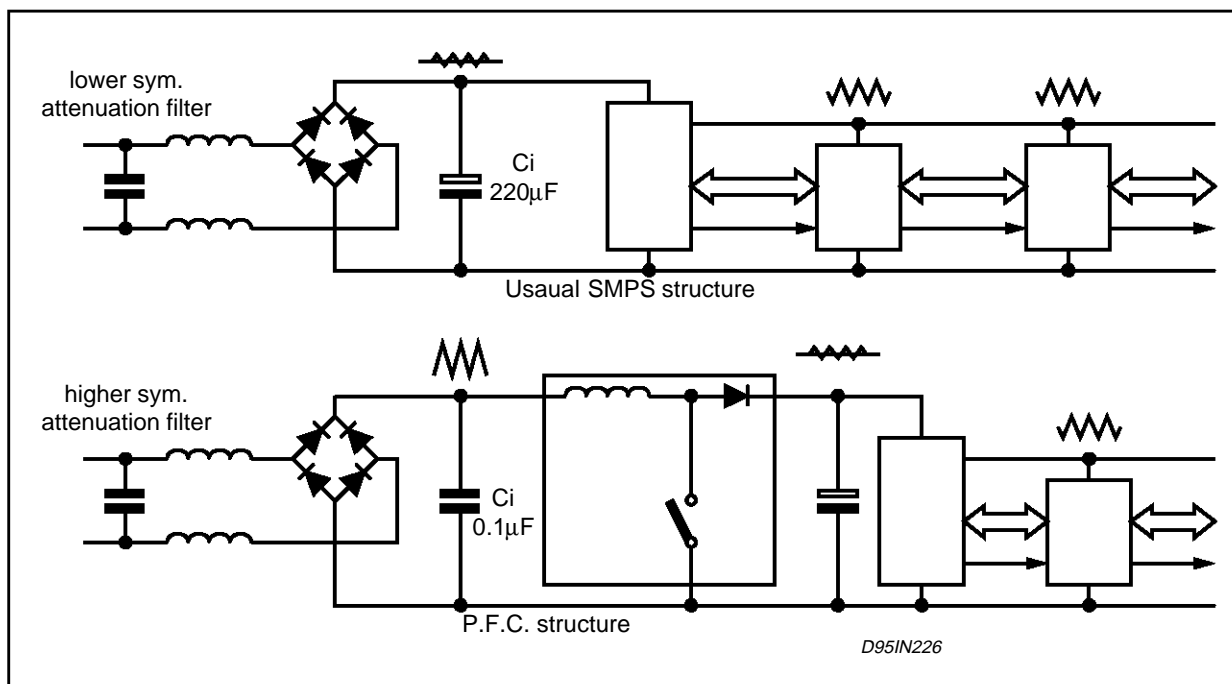
The PFC also provides additional functions such as automatic mains voltage selection and a constant output voltage.

Nevertheless, size a nd cost optimization of PFC has to take the RFI filter section into account.

A PFC circuit generates more high frequency interferences to the mains than a conventional rectifier front-end section (see figure 5).

The PFC use requires thus additional filtering. For this reason, modulation techniques and mode of operation for the PFC have to be carefully adapted to the application requirement.

Figure 5: A Power Factor Converter generates higher frequency interferences to the mains than a conventional rectifier front-end

lower sym. attenuation filter

Ci 220μF

Usaual SMPS structure

higher sym. attenuation filter

Ci 0.1μF

P.F.C. structure

D95IN226

SGS-THOMSON MICROELECTRONICS

SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.

SGS-THOMSON
MICROELECTRONICS